Remarks:

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Status of Claims

Claims 1 – 23 and 27 – 43 are pending in the application. Claims 1 – 23 and 27 – 43 have been rejected.

Claims 4 – 5, 9, 11, 13 – 18, 29, 31 and 33 – 38 have been cancelled without prejudice. Applicants reserve the right to present the subject matter of the cancelled claims in a divisional or continuation application.

Claims 1, 8, 12, 27, 30 and 43 have been amended. New claims 44 – 54 have been added. No new matter has been added.

35 U.S.C. 102 Rejections

The Office Action rejects claims 1 – 23 and 27 – 43 under 35 U.S.C. 102(e) as being anticipated by US 5,987,490 (Alidina et al.). Applicants respectfully traverse the rejection, in view of the remarks that follow.

> As is well established, in order to successfully assert a *prima facie* case of anticipation, the Examiner must provide a single prior art document that includes every element and limitation of the claim or claims being rejected.
>
> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (MPEP 2131)

Alidina et al. discloses "a pair of adder arithmetic logic units ... supporting full and split-mode" (abstract). Alidina et al. does not disclose, either expressly or inherently, *"no more than one arithmetic logic unit operating in split mode"*, as recited by amended claim 1. Therefore, Alidina et al. cannot anticipate claim 1 as amended. Claims 2, 3, 6 and 7 are

dependent from claim 1 and include all the limitations of the independent claim. Therefore, Alidina et al. cannot anticipate claims 2, 3, 6 and 7.

Claim 8 as amended recites *"a storage device having memory cells, wherein a group of at least one memory cell is to store all trace bits for a stage of Viterbi decoding of a binary convolution code in sequential order"*. Alidina et al. discloses storing trace bits in registers ar0 and ar1 but does not disclose, either expressly or inherently, a single storage device to store all trace bits for a stage. Therefore, Alidina et al. cannot anticipate claim 8 as amended. Claim 10 is dependent from claim 8 and includes all the limitations of the independent claim. Therefore, Alidina et al. cannot anticipate claim 10.

Claim 12 as amended recites similar limitations to those of claim 8 as well as additional limitations. Therefore Alidina et al. cannot anticipate claim 12.

According to Alidina et al, the traceback output is shifted into two separate registers ar0 and ar1.

Alidina et al. does not disclose *"a storage device having memory cells, wherein for each of said multiple stages, a group of one or more memory cells is to store said trace bits in sequential order"*, as recited by claim 19. Therefore Alidina et al. does not disclose all the limitations of claim 19 and its dependent claims 20 – 23. Consequently, the Office Action has failed to establish a prima facie case of anticipation regarding claims 19 – 23.

Alidina et al. does not disclose *"saving said trace bits in sequential order to a group of one or more memory cells"* as recited by amended claim 27. Therefore Alidina et al. cannot anticipate claim 27 as amended. Claims 28, 30 and 32 are dependent from claim 27 and include all the limitations of the independent claim. Therefore Alidina et al. cannot anticipate claims 28, 30 and 32.

Alidina et al. does not disclose *"for each of said multiple stages, storing said trace bits in sequential order in a group of one or more memory cells"*, as recited by claim 39. Therefore Alidina et al. does not disclose all the limitations of claim 39 and its dependent claims 40 – 43. Consequently, the Office Action has failed to establish a prima facie case of anticipation regarding claims 39 – 43.

Remarks to New Claims

As required by 37 CFR 1.111(c), the following remarks clearly point out the patentable novelty which Applicant thinks the newly added claims 44 – 54 present in view of the state of the art disclosed by the references cited.

Alidina et al. discloses that the "generated traceback output is shifted into a traceback register for later use in a Viterbi traceback routine" (abstract). However, Alidina et al. is silent as to any features of the Viterbi traceback routine.

Alidina et al. does not disclose, either expressly or inherently, *"tracing back, stage by stage, in as few as two clock cycles per stage, states of binary convolution codes that are decoded using Viterbi decoding"*, as recited by new claim 44. Therefore Alidina et al. cannot anticipate claim 44 and its dependent claims 45 – 50.

Alidina et al. does not disclose, either expressly or inherently, *"generating a generated B-bit binary representation having a least significant bit equal to a trace bit of a state of a particular stage and having (B-1) most significant bits equal to the (B-1) least significant bits of a B-bit binary representation of an index of said state ... wherein B is the integer part of the logarithm to base 2 of the number of states in a stage"*, as recited by new claim 51. Therefore Alidina et al. cannot anticipate claim 51 and its dependent claims 52 – 53.

Alidina et al. does not disclose, either expressly or inherently, "a memory element to store in its B least significant bits a B-bit binary representation of an index of a state of a stage, where B is the integer part of the logarithm to base 2 of the number of said states", as recited by new claim 54. Therefore Alidina et al. cannot anticipate claim 54.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Respectfully submitted,

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